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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/599,783	06/22/2000	Toshiharu Furukawa	BU9-99-197	7947

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EXAMINER
MALDONADO, JULIO J

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/599,783	FURUKAWA ET AL.
	Examiner	Art Unit
	Julio J. Maldonado	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 June 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,8-12,14-21,24-28 and 30-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,8-10,12,14-18,21,24,25,28 and 30-32* is/are rejected.

7)☒ Claim(s) *3,4,11,19,20,26 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 5, 6, 15-18, 21, 24, 25, 28, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koch et al. (U.S. 5,413,884) in view of Angelopoulos et al. (6,316,167 B1).

In reference to claims 1, 2, 5, 15, 17, 18, 21, 24, 25, 31 and 32, Koch et al. (Figs.7-11) in a related method to etch a substrate teach the steps of depositing a layer of metallic germanium (44) over a dielectric layer (42); patterning the layer of metallic germanium (44) to form the germanium hard mask as a top most layer over the dielectric layer (42) by depositing a photo resist layer (46) over the layer of metallic germanium (44), exposing and developing the photo resist layer (46) to form a photolithography image (50) and etching the layer of metallic germanium (44) through the photolithography image (50); selectively etching the dielectric layer (42) through the germanium hard mask (44) as a to form an opening in the dielectric layer (42); striping away the layer of metallic germanium (44); and selectively etching the semiconductor substrate (32) through the opening in the dielectric layer (42) (column 5, line 26 – column 6, line 27).

Koch et al. fail to teach forming a dielectric stack over the substrate and removing the photo resist prior to selectively etching the dielectric stack through the germanium hard mask. However, Angelopoulos et al. (Fig.11) in a related method to etch a semiconductor substrate teach forming a dielectric stack over the substrate and removing a photo resist layer prior to etch the dielectric stack (column 14, lines 11-39). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a dielectric stack as taught by Angelopoulos et al. in the etching process of Koch et al., since this would improve etch performance needed for the transfer of the resist pattern through the substrate (column 3, lines 23-38). Also, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to remove the photoresist layer prior (i.e. reducing the thickness) to etch the dielectric stack as taught by Angelopoulos et al. in the etching process of Koch et al., since this would allow better resolution to the transferred lithograph (column 3, lines 20-23).

In reference to claims 6, 16, and 28, Koch et al. in combination with Angelopoulos et al. teach patterning the layer of metallic germanium to form the germanium hard mask (Koch et al., Fig.9) but fail to show said layer having a thickness between approximately 40 nm and approximately 500 nm. However, the selection of the claimed range is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general

conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

3. Claims 8 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koch et al. ('884) in view of Angelopoulos et al. ('167 B1) as applied to claims 1, 2, 5, 6, 15-18, 21, 24, 25, 28 31 and 32 above, and further in view of Cho et al. (U.S. 6,074,930).

Koch et al. in combination with Angelopoulos et al. using a dielectric stack comprised of bi-layers and tri-layer to etch the semiconductor substrate (Angelopoulos et al., column 3, lines 31-45). Koch et al. in combination with Angelopoulos et al. fail to teach a dielectric stack comprising a pad oxide having a thickness between approximately 5 nm and 30 nm, a nitride layer having a thickness between approximately 50 nm and 300 nm and a mask oxide having a thickness between approximately 800 nm and 3,000 nm. However, Cho et al. (Figs.4-12) in a related method to form a trench in a semiconductor substrate teach forming a dielectric stack comprising a pad oxide (32), a nitride layer (34) and a mask oxide layer (36) (column 3, line 61 – column 4, line 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a tri-layer mask comprised of a pad oxide, a nitride layer and a mask oxide as taught by Cho et al. in the combination of Koch et al. and Angelopoulos et al., since the formation of such layers in the fabrication of trenches in a semiconductor substrate involves ordinary skill in the art (column 1, lines 36-48).

Still, the combined teachings of Koch et al., Angelopoulos et al. and Cho et al. fail to teach forming the pad oxide having a thickness between approximately 5 nm and 30 nm, forming the nitride layer having a thickness between approximately 50 nm and 300 nm and forming the mask oxide having a thickness between approximately 800 nm and 3,000 nm. However, the selection of the claimed ranges is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

4. Claims 9, 10, 12, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koch et al. ('884) in view of Angelopoulos et al. ('167 B1) and Cho et al. ('930).

Koch et al. (Figs.7-11) in a related method to etch a semiconductor substrate teach the steps of depositing a layer of metallic germanium (44) over a dielectric layer (42); patterning the layer of metallic germanium (44) to form the germanium hard mask as a top most layer over the dielectric layer (42) by depositing a photo resist layer (46) over the layer of metallic germanium (44), exposing and developing the photo resist layer (46) to form a photolithography image (50) and etching the layer of metallic germanium (44) through the photolithography image (50); selectively etching the dielectric layer (42) through the germanium hard mask (44) as a to form an opening in the dielectric layer (42); striping away the layer of metallic germanium (44); and

selectively etching the semiconductor substrate (32) through the opening in the dielectric layer (42) (column 5, line 26 – column 6, line 27).

Koch et al. fail to teach forming a dielectric stack over the substrate and removing the photo resist prior to selectively etching the dielectric stack through the germanium hard mask. However, Angelopoulos et al. (Fig.11) in a related method to etch a semiconductor substrate teach forming a dielectric stack over the substrate and removing a photo resist layer prior to etch the dielectric stack (column 14, lines 11-39). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a dielectric stack as taught by Angelopoulos et al. in the etching process of Koch et al., since this would improve etch performance needed for the transfer of the resist pattern through the substrate (column 3, lines 23-38). Also, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to remove the photoresist layer prior (i.e. reducing the thickness) to etch the dielectric stack as taught by Angelopoulos et al. in the etching process of Koch et al., since this would allow better resolution to the transferred lithograph (column 3, lines 20-23).

Still, the combination of Koch et al. and Angelopoulos et al. fail to teach the steps of forming doped regions in the semiconductor substrate and forming dielectric and conductive structures over the semiconductor substrate and providing a dielectric stack comprising a pad oxide, a nitride layer, and a mask oxide layer. However, Cho et al. (Figs.4-12) in a related method to form a trench structure in a semiconductor substrate teach the steps of doped regions in the semiconductor substrate (30) and forming

dielectric and conductive structures over the semiconductor substrate, and providing a dielectric stack comprising a pad oxide (32), a nitride layer (34) and a mask oxide layer (36) (column 1, lines 15-23 and column 3, line 61 – column 4, line 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to dope regions and form dielectric and conductive devices as taught by Cho et al. in the combination of Koch et al. and Angelopoulos et al., since the formation of dielectric and conductive structures in the semiconductor substrate involves routine skill in the art (column 1, lines 15-48).

Still, the combined teachings of Koch et al., Angelopoulos et al. and Cho et al. fail to teach forming the germanium layer having a thickness between approximately 40 nm and 500 nm. However, the selection of the claimed ranges is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species. In re Jones, 162 USPQ 224 (CCPA 1955)(the selection of optimum ranges within prior art general conditions is obvious) and In re Boesch, 205 USPQ 215 (CCPA 1980)(discovery of optimum value of result effective variable in a known process is obvious).

Allowable Subject Matter

5. Claims 3, 4, 11, 19, 20, 26 and 27 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter:

Koch et al. (Figs.7-11) in a related method to etch a semiconductor substrate teach the steps of depositing a layer of metallic germanium (44) over a dielectric layer (42); patterning the layer of metallic germanium (44) to form the germanium hard mask as a top most layer over the dielectric layer by depositing a photo resist layer (46) over the layer of metallic germanium (44), exposing and developing the photo resist layer (46) to form a photolithography image (50) and etching the layer of metallic germanium (44) through the photolithography image (50); selectively etching the dielectric layer (42) through the germanium hard mask (44) as a to form an opening in the dielectric layer (42); striping away the layer of metallic germanium (44); and selectively etching the semiconductor substrate (32) through the opening in the dielectric layer (42) (column 5, line 26 – column 6, line 27).

However, Koch et al. fails to teach stripping away the germanium layer from the dielectric stack by oxidizing the germanium layer, transforming it to germanium oxide and rinsing the germanium oxide layer with water.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted directly to Art Unit 2823 by facsimile transmission. Papers should be faxed to Art Unit 2823 via the Art Unit 2823 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2823 Fax Center number is **(703) 305-3432**. The Art Unit 2823 Fax Center is to be used only for papers related to Art Unit 2823 applications.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Julio J. Maldonado** at **(703) 306-0098** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via julio.maldonado@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (703) 308-4918.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

Wael Fahmy

SUPERVISORY PRIMARY EXAMINER
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